Amendments to the Claims/Listing of Claims

1. (Previously presented) A method for programming a field mounted device having a memory, the method comprising the steps of:

running a computational process having data read access to an activated first memory area storing a programmable first device configuration;

C1 deactivating the first memory area during on-line operation of the device, wherein said step comprises precluding said computational process to access the first memory area; and

activating a deactivated second memory area storing a programmable second device configuration during on-line operation of the device, wherein said step comprises granting said computational process data read access to the second memory area.

2. (Original) The method of claim 1, further comprising the steps of:

running a first configuration process having data read and write access to the deactivated second memory area; and

storing data in the second memory area for modifying the second device configuration in the second memory area.

3. (Original) The method of claim 2, further comprising the step of

executing the first device configuration in the first memory area by the computational process during running the first configuration process.

4. (Original) The method of claim 2, further comprising the steps of:

running a second configuration process having data read and write access to a deactivated third memory area; and

storing data in the third memory area.

5. (Previously presented) The method of claim 4, further comprising the steps of:

precluding the second configuration process access to the second memory area by granting the first configuration process an exclusive access to the second memory area;

modifying via said second configuration process the second device configuration in the second memory area; and

granting the computational process access to the second memory area after said modifying step.

6. (Original) The method of claim 2, further comprising the step of

storing the first device configuration into the second memory area.

7. (Original) The method of claim 1, further comprising the steps of:

writing over a first branch address that references the first memory area with a second branch address that references the second memory area for deactivating the first memory area and activating the second memory area in a single write access.

8. (Original) The method of claim 7, further comprising the steps of:

deactivating the first memory area upon the occurrence of a hardware or software error in the first memory area; and

activating the second memory area upon said occurrence of said error.

9. (Original) The method of claim 7, further comprising the step of

copying the first device configuration from the first memory area into the second memory area.

10. (Original) The method of claim 9, further comprising the step of

executing the first device configuration in the first memory area by the computational process during the copying step.

11. (Previously presented) A programmable field mounted device, comprising:

a memory circuit including a plurality of memory areas, each memory area storing program codes, each memory area selectively activated;

a control circuit configured to generate a selection signal, the selection signal activating one of the plurality of memory areas during on-line operation of the device to create an activated memory area containing a first program code representing a first device configuration, and deactivating the one of the remaining memory areas during on-line operation of the device to create a deactivated memory area for storing a second program code representing a second device configuration.

12. (Previously presented) The device of claim 11, wherein the control circuit includes a microprocessor, the microprocessor having read access to the activated memory area for executing the first program code.

13. (Original) The device of claim 11, further comprising a configuration device configured to modify the second program code in the deactivated memory area.

14. (Previously presented) The device of claim 13, wherein the control circuit is configured to grant the configuration device read and write access to the deactivated memory area for modifying the second program code.

15. (Original) The device of claim 11, wherein the control circuit is further configured to deactivate the activated memory area containing the first program code and

activate the deactivated memory area containing the modified second program code.

16. (Previously presented) The device of claim 12, wherein the control circuit is further configured to provide the microprocessor read access to the memory area containing the second program code for executing the second program code.

17. (Previously presented) The device of claim 11, wherein the deactivated memory area containing the second program code is activated by writing in the memory circuit a branch address corresponding to said memory area.

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18. (Previously presented) The device of claim 11, wherein the activated memory area containing the first program code is deactivated by writing over a branch address in the memory circuit corresponding to said memory area address with the branch address corresponding to the memory area containing the second program code.

19. (Original) The device of claim 11, wherein the memory circuit is a non-volatile memory.

20. (Original) The device of claim 11, wherein the memory circuit is an EEPROM.

21. (Original) The device of claim 11, further including an energy storage device configured to store energy for at least one write access to the memory circuit.

22. (Currently amended) A method for programming a field mounted device running a computational process, the method comprising the steps of:

activating a first memory area storing a first programmable configuration;

deactivating a second memory area storing a second programmable configuration;

configuring the second memory area with a modification of the second programmable configuration; and

coordinating the configuration of the second memory area during on-line operation of said device with the computational process, the coordination of the configuration of the second memory area including the steps of simultaneously executing the first programmable configuration in the first memory area by the computational process during configuration of the second memory area with a modification of the second programmable configuration, deactivating the first memory area storing the first programmable configuration upon completion of configuring the second memory area with a modification of the second programmable configuration, and activating the second memory area upon completion of configuring the second memory area with a modification of the second programmable configuration.

23. (Original) The method of claim 22, wherein the step of activating the second memory area and deactivating the first memory area comprises the step of writing over a first branch address that references the first memory with a second branch address that references the second memory area.

24. (Original) The method of claim 22, wherein the step of coordinating the configuration of the second memory area with the computational process further comprises the steps of:

precluding the computational process access to the second memory area;

granting a configuration process exclusive access to the second memory area; and

granting the computation process access to the second memory area after the modifying step.

25. (Original) The method of claim 22, wherein the step of activating the second memory area and deactivating the first memory area is accomplished by a single write access to a branch address.

26. (Previously presented) The device of claim 15, wherein the control circuit is further configured to provide the microprocessor read access to the memory area containing the second program code for executing said program code.

27. (Currently amended) A method for reconfiguring a programmable field mounted device during on-line operation of said field mounted device, said field mounted device including field mounted device electronics and said field mounted device sending data to a process monitoring system via a data transmission system, said method comprising the steps of:

running via a microprocessor of said field mounted device electronics a computational process executing a first program code stored in a data memory circuit of said field mounted device electronics, said first program code representing a first configuration of said field mounted device and said first program code being stored within a first memory area of said data memory circuit;

transferring to a second memory area of the data memory circuit ~~said field mounted device~~ a second program code representing a second configuration of said field mounted device, said second memory area being deactivated to preclude said computational process to access the second memory area;

using said modification data to write data to said data memory circuit, said data representing said second program code;

terminating the transfer of modification data;

activating the second memory area to grant said computational process to access said second memory; and

executing via the microprocessor said second program code;

wherein the step of transferring to said field mounted device said second program code comprises a step of sending modification data from an external programming device via said data transmission system to said field mounted device during running said computational process.

28. (Previously presented) The method as claimed in claim 27, wherein the data memory circuit comprises a second memory area, said method further comprising a step of deactivating said second memory area of said data memory circuit to preclude said computational process to access said second memory area.

29. (Previously presented) The method as claimed in claim 28, wherein said step of executing via the microprocessor said second program code comprises a step of activating said second memory area of said data memory circuit to grant said computational process data read access said second memory area.

30. (Previously presented) The method as claimed in claim 29, further comprising a step of deactivating said first memory area of said data memory circuit to preclude said computational process data read access said first memory area.

31. (Previously presented) The method as claimed in claim 27, further comprising a step of using a sensor being connected with said field mounted device electronics for sensing a process variable from a process to be monitored using said field mounted device.

32. (Previously presented) The method as claimed in claim 31, further comprising a step of generating a measurement signal representing said process variable.

33. (Previously presented) The method as claimed in claim 32, wherein the field mounted device electronics further comprises a communication interface coupled to said data transmission system, said method further comprising a step of using said communication interface to send said measurement signal to said process monitoring system.